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**SUPERLATTICE NANOPATTERNING OF
WIRES AND COMPLEX PATTERNS**

**STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR
DEVELOPMENT**

[0001] This invention was made with support from the Defense Advanced Research Projects Agency (DARPA) Grant #MDA972-01-3-0005. The government has certain rights in this invention.

This application is a 371 of PCT/US03/23546 filed 07/28/2003

BACKGROUND OF THE INVENTION

1. **Field of the Invention**

[0002] The present invention involves the production of electronic and mechanical devices with length scales measured in nanometers to microns. More particularly, the invention encompasses complicated electrical circuits, mechanical devices, and spatially modulated physical properties. Currently, similar devices (with larger feature sizes) are fabricated using photolithography and related processes often employed by the semiconductor industry.

2. **Description of Related Art**

[0003] The silicon integrated circuit industry (IC) has dominated electronics and has helped it grow to become one of the world's largest and most critical industries over the past thirty-five years. However, because of a combination of physical and economic reasons, the miniaturization that has accompanied the growth of Si IC's is reaching its limit. The present scale of devices is on the order of tenths of micrometers. New solutions are being proposed to take electronics to even smaller levels; such solutions are directed to constructing nanometer scale devices.

[0004] Prior proposed solutions to the problem of constructing nanometer scale devices have involved (1) utilization of extremely fine scale lithography using X-rays, electrons, ions, or scanning probes to define the device components; (2) direct writing of the device components by electrons, ions, or scanning probes, or (3) using a master fabricated with either process (1) or (2) to stamp the device components into a conformal layer. The major problem with (1) is the capital expense necessary